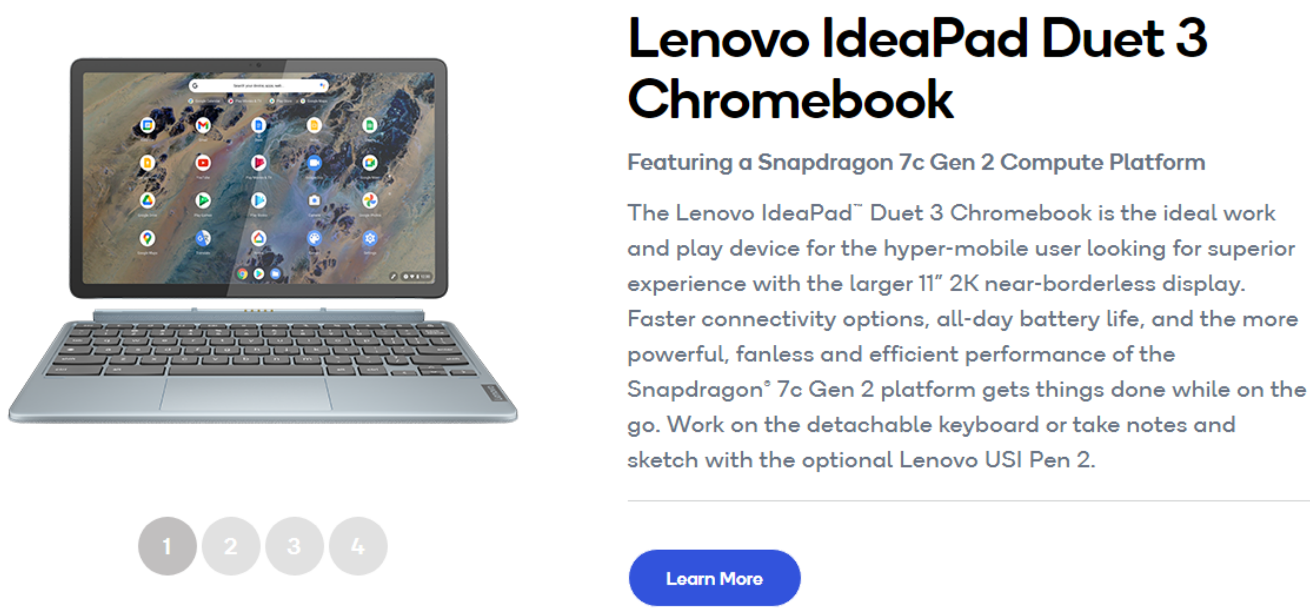
EXHIBIT 028

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
“Integrated circuit and method of communication service mapping”

<table>
<tr><th>’052 Patent Claim</th><th>Lenovo Product Including Snapdragon System on Chip[1]</th></tr>
<tr><td>6. Method of communication service mapping in an integrated circuit, having a plurality of processing modules (M, S),</td><td>

Without conceding that the preamble of claim 6 of the ‘052 Patent is limiting, the Lenovo IdeaPad Duet 3 Chromebook (hereinafter, the “Lenovo product”) performs a method of communication service mapping in an integrated circuit, having a plurality of processing modules (M, S), either literally or under the doctrine of equivalents.

The Lenovo product includes an integrated circuit. For example, the Lenovo product includes the Qualcomm Snapdragon 7c Gen 2 Compute Platform system on chip (hereinafter, the “Snapdragon SoC”).



</td></tr>
</table>

[1] The Lenovo product is charted as a representative product made used, sold, offered for sale, and/or imported by Lenovo. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein.

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	https://www.qualcomm.com/products/application/mobile-computing/laptop-device-finder/lenovo-ideapad-duet-3-chromebook The Snapdragon SoC comprises a plurality of processing modules (M, S), for example Qualcomm Adreno GPU; Octa-core Qualcomm Kryo 468 CPU; and Qualcomm Hexagon 692 DSP:

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	Qualcomm® Snapdragon™ 7c Gen 2 Compute Platform Specifications & Features **CPU** • CPU Clock Speed: Up to 2.55 GHz • CPU Cores: Octa-core Qualcomm® Kryo™ 468 CPU • CPU Architecture: 64-bit **Process** • Process Technology: 8 nm **OS Support** • Supports Windows 10 and Windows 11 • Chrome OS **Memory** • Memory Type: 2 x 16-bit, LPDDR4x-4266 **Storage** • UFS: eMMC 5.1; UFS 2.1 **Visual Subsystem** • GPU: Qualcomm® Adreno™ GPU **Camera** • Image Signal Processor: Qualcomm Spectra™ 255 image signal processor, 14-bit • Dual Camera, ZSL, 30fps: Up to 16 MP **Video** • Video Playback: Up to 4K HDR10 • Codec Support: H.265 (HEVC), H.264 (AVC), VP9 • Video Software: Motion Compensated Temporal Filtering (MCTF) **Display** • Max On-Device Display: QXGA @ 60Hz, FHD @ 60Hz • Max External Display: QHD @ 60Hz • Display Pixels: 2560x1440, 2048x1536 **General Audio** • Qualcomm Aqstic technology: Qualcomm Aqstic™ audio codec, Qualcomm Aqstic smart speaker amplifier • Qualcomm® aptX™ audio playback support: aptX, aptX HD **Audio Playback** • PCM, Playback: Up to 384kHz/32bit • Additional Playback Features: Native DSD support **Qualcomm® AI Engine** • AIE CPU: Octa-core Kryo 468 CPU • Uplink Technology: Qualcomm® Snapdragon™ Upload+ • Uplink Carrier Aggregation: 2x20 MHz carrier aggregation • Uplink QAM: Up to 64-QAM • LTE Speed • LTE Peak Download Speed: 600 Mbps **Wi-Fi** • Wi-Fi Standards: 802.11ac Wave 2, 802.11a/b/g, 802.11n • Wi-Fi Spectral Bands: 2.4 GHz, 5 GHz • MIMO Configuration: 2x2 (2-stream) • Qualcomm® FastConnect™ Subsystem **Bluetooth Version** • Bluetooth 5.0 **GPS Location** • Satellite Systems Support: NavIC, BeiDou, Galileo, GLONASS, GPS, QZSS, SBAS **Security** • Qualcomm® Processor Security • Qualcomm® Content Protection • Wi-Fi Security: WPA3

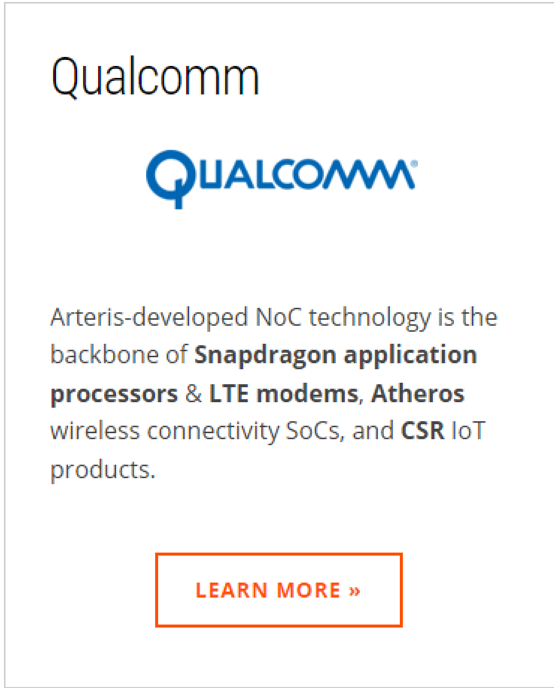
4893-4043-7313.3

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	Camera • Image Signal Processor: Qualcomm Spectra™ 255 image signal processor, 14-bit • Dual Camera, ZSL, 30fps: Up to 16 MP • Single Camera, ZSL, 30fps: Up to 32 MP • Camera Features: Multi-frame Noise Reduction (MFNR) • Video Capture Features: Rec. 2020 color gamut video capture, Up to 10-bit color depth video capture **CAMERA FEATURES** • Advanced DPD, WPA3 • Multi-Frame Noise Reduction (MFNR) and Multi-Frame Super Resolution (MFSR) • Forward-looking Electronic Image Stabilization (EIS) • Motion Compensated Temporal filtering (MCTF) for noise-free video capture up to UHD (4K) at 30 FPS • Four MIPI CSI PHYs (DPHY 1.2 / CPHY 1.2) • Additional Playback Features: Native DSD support **Qualcomm® AI Engine** • AIE CPU: Octa-core Kryo 468 CPU • AIE GPU: Adreno GPU • AIE DSP: Qualcomm® Hexagon™ 692 DSP **Cellular Modem** • Modem Name: Snapdragon X15 LTE modem • LTE Category • Downlink LTE Category: LTE Category 12 • Uplink LTE Category: LTE Category 13 • LTE Downlink Features • Downlink Carrier Aggregation: 3x20 MHz carrier aggregation • Downlink LTE MIMO: Up to 4x4 MIMO on two carriers • Downlink QAM: Up to 256-QAM, Up to 64-QAM • LTE Uplink Features • Qualcomm® Processor Security • Qualcomm® Content Protection • Wi-Fi Security: WPA3 https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/prod_brief_qcom_sd7c_gen2.pdf The Snapdragon SoC included in the Lenovo product utilizes Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the "Arteris NoC") for communication service mapping:

4893-4043-7313.3

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

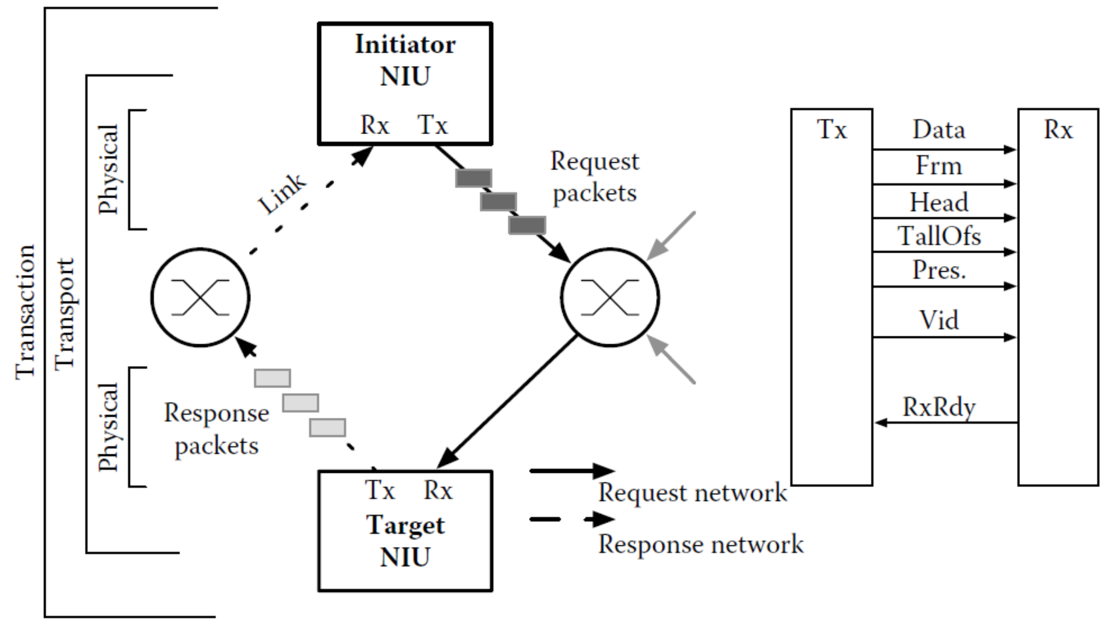
'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	 https://web.archive.org/web/20210514110614/https://www.arteris.com/customers

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	Certain Arteris Technology Assets Acquired by **Kurt Shuler**, on October 31, 2013 Arteris to continue to license, support and maintain Arteris FlexNoC® interconnect IP SUNNYVALE, California — October 31, 2013 — Arteris Inc., a leading innovator and supplier of silicon-proven commercial network-on-chip (NoC) interconnect IP solutions, today announced that Qualcomm Technologies, Inc. ("Qualcomm"), a subsidiary of Qualcomm Incorporated, has acquired certain technology assets from Arteris and hired personnel formerly employed by Arteris. *Arteris NoC technology has been and will continue to be a key enabler for creating larger and more complex chips in a shorter amount of time at a lower cost. This acquisition of our technology assets represents a validation of the value of Arteris' Network-on-Chip interconnect IP technology.* ARTERIS IP *K. Charles Janac, President and CEO, **Arteris*** https://www.arteris.com/press-releases/Qualcomm-Arteris-asset-acquisition-2013_oct_31; https://www.fiercewireless.com/tech/qualcomm-acquires-arteris-noc-tech-assets-team The Arteris NoC performs communication service mapping in the Snapdragon SoC included in the Lenovo product. For example, the Arteris NoC uses Network Interface Units (NIUs), which "translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols" and in the Arteris NoC "[m]ost transactions require the following two-step transfers," including "[a] master send[ing] request packets" and "the slave return[ing] response packets":

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	11.3.1.1 Transaction Layer The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	 **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313; *see id* at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: "In this chapter we will present an MPSoC platform […] using Arteris NoC as communication infrastructure.").
wherein at least one first of said processing modules (M) requests at least	Without conceding that the preamble of claim 6 of the '052 Patent is limiting, at least one first of said processing modules (M) of the Snapdragon SoC included in the Lenovo product utilizes the Arteris NoC to request at least one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification wherein said at least one communication service identification comprises at least

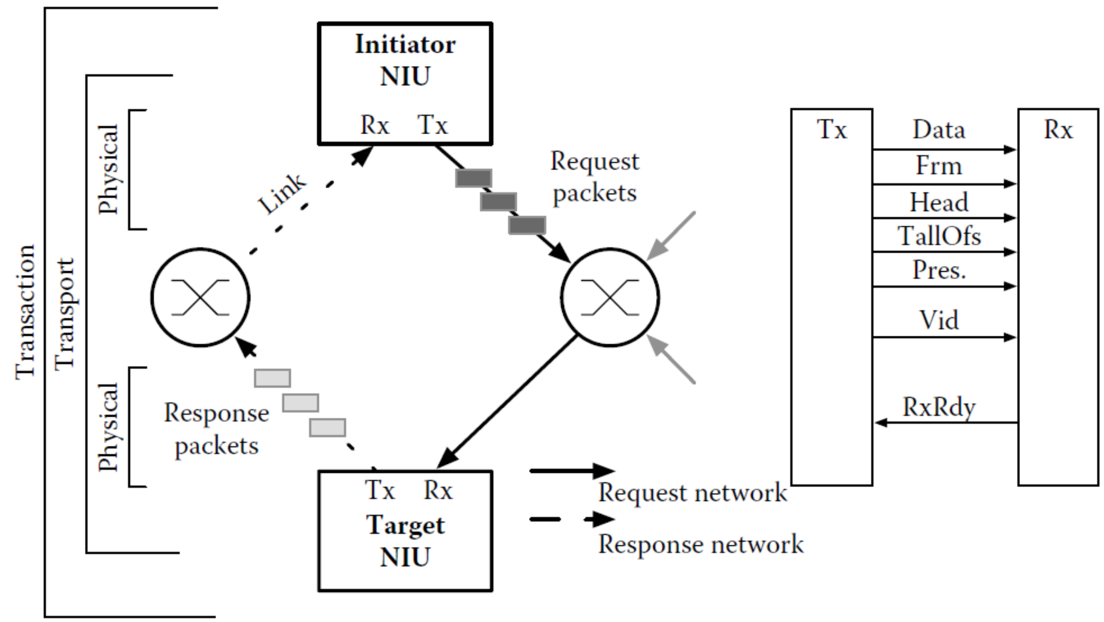
4893-4043-7313.3

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
one communication service to at least one second processing module (S) based on specific communication properties and at least one communication service identification, wherein said at least one communication service identification comprises at least one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region	one communication thread or at least one address range, said address range for identifying one or more second processing modules (S) or a memory region within said one or more second processing modules (S), either literally or under the doctrine of equivalents. For example, the Arteris NoC utilized by the Snapdragon SoC included in the Lenovo product uses Network Interface Units (NIUs), which "translate[] between third-party [OCP, AMBA AHB, APB, and AXI protocols] and NTTP protocols" and in the Arteris NoC, "[m]ost transactions require the following two-step transfers," including "[a] master send[ing] request packets" and "the slave return[ing] response packets": ***11.3.1.1 Transaction Layer*** The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
within said one or more second processing modules (S),	on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network.

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	 **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313. The "Arteris NTTP protocol is packet-based" and the packets, which have "header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address," are "transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes":

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	11.3.1.2 Transport Layer The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target. *Id.* at 313. As yet a further illustration, packets in the Arteris NoC are "delivered as words that are sent along links and "[o]ne link (represented in Figure 11.1) defines the following signals," which include "the current priority of the packet used to define preferred traffic class (or Quality of Service)" and "[f]low control":

	maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in Figure 11.1) defines the following signals: • **Data**—Data word of the width specified at design-time. • **Frm**—When asserted high, indicates that a packet is being transmitted. • **Head**—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only. • **TailOfs**—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only. • **Pres.**—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2). • **Vld**—Data valid: when asserted high, indicates that a word is being transmitted. • **RxRdy**—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy. This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTTP communications.

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	Id. at 313-314. As a further example, the packets sent in the Arteris NoC are "composed of cells that are organized into fields, with each field carrying specific information," including "Pres," "Slave address" and "Slave offset":

Field	Size	Function
Opcode	4 bits/3 bits	Packet type: 4 bits for requests, 3 bits for responses
MstAddr	User Defined	Master address
SlvAddr	User Defined	Slave address
SlvOfs	User Defined	Slave offset
Len	User Defined	Payload length
Tag	User Defined	Tag
Prs	User defined (0 to 2)	Pressure
BE	0 or 4 bits	Byte enables
CE	1 bit	Cell error
Data	32 bits	Packet payload
Info	User Defined	Information about services supported by the NoC
Err	1 bit	Error bit

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]

StartOfs	2 bits	Start offset
StopOfs	2 bits	Stop offset
WrpSize	4 bits	Wrap size
Rsv	Variable	Reserved
CtlId	4 bits/3 bits	Control identifier, for control packets only
CtlInfo	Variable	Control information, for control packets only
EvtId	User defined	Event identifier, for event packets only

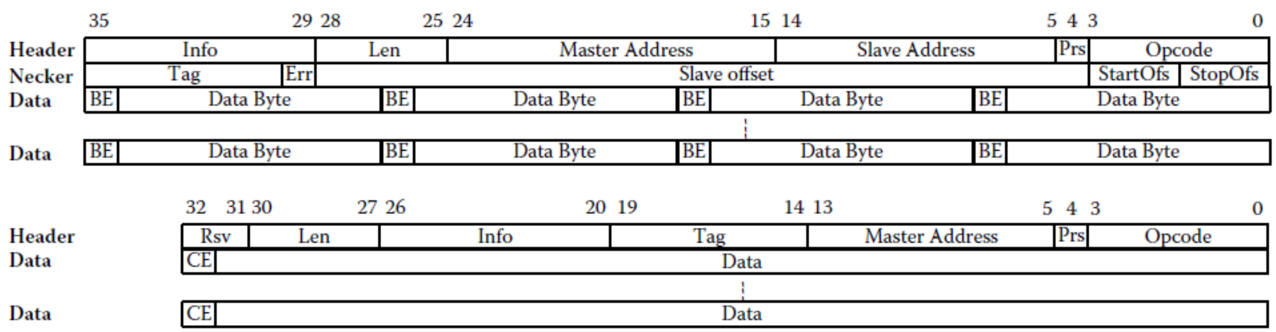


FIGURE 11.2
NTTP packet structure.

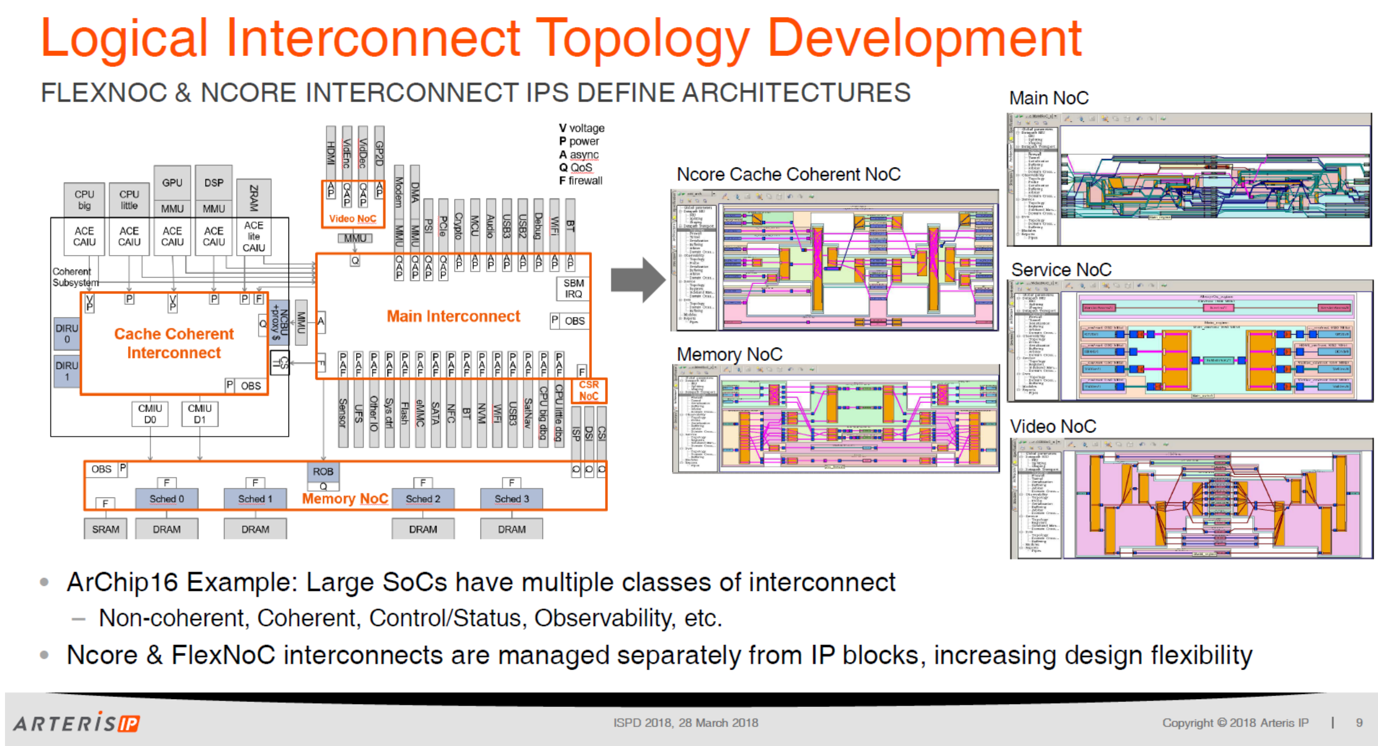
Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313, 314-315.

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	As further illustration, "[f]or the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2)." *Id.* at 318.
comprising the steps of: coupling said plurality of processing modules (M, S) by an interconnect means (N) and enabling a connection based communication having a set of connection properties,	The Arteris NoC utilized by the Snapdragon SoC included in the Lenovo product couples the plurality of processing modules (M, S) by an interconnect means (N) and enables a connection based communication having a set of connection properties, either literally or under the doctrine of equivalents. The Arteris NoC couples the plurality of processing modules in the Snapdragon SoC included in the Lenovo product by an interconnect means. A large SoC, such as the Snapdragon SoC included in the Lenovo product may include multiple classes of Arteris NoC interconnect:

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]

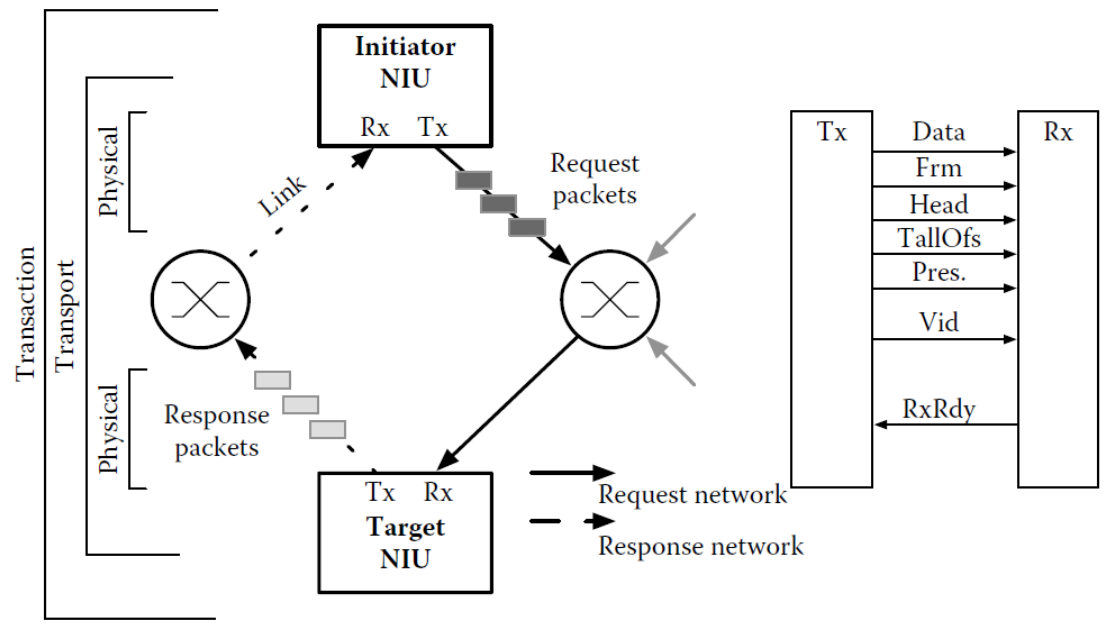


See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 9.

The Arteris NoC enables a connection based communication having a set of connection properties.

For example, in the Arteris NoC, "[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network…. Transactions are handed off to the transport layer, which is responsible for delivering

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path."  **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313.

4893-4043-7313.3

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	The "Arteris NTTP protocol is packet-based" and the packets, which have "header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address," are "transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes": ***11.3.1.2 Transport Layer*** The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target. *Id.* at 313. As a further illustration, packets in the Arteris NoC are "delivered as words that are sent along links and "[o]ne link (represented in Figure 11.1) defines the following signals," which include "the current priority of the packet used to define preferred traffic class (or Quality of Service)" and "[f]low control":

	maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in Figure 11.1) defines the following signals: • **Data**—Data word of the width specified at design-time. • **Frm**—When asserted high, indicates that a packet is being transmitted. • **Head**—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only. • **TailOfs**—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only. • **Pres.**—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2). • **Vld**—Data valid: when asserted high, indicates that a word is being transmitted. • **RxRdy**—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy. This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTTP communications.

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	Id. at 313-314. As yet a further illustration, the Arteris NoC implements Quality of Service (QoS) to "provide[] a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic"; QoS, which includes guarantees of, for example, throughput and/or latency, "is achieved by exploiting the signal pressure embedded into the NTTP packet definition" where the "pressure signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed"; and the "pressure information will be embedded in the NTTP packet at the NIU level": **Quality of Service (QoS).** The QoS is a very important feature in the interconnect infrastructures because it provides a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic. Usually the end users are looking for guarantees on bandwidth and/or end-to-end communication latency. Different mechanisms and strategies have been proposed in the literature. For instance, in Æthereal NoC [11,24] proposed by NXP, a TDMA approach allows the specification of two traffic categories [25]: BE and GT. In the Arteris NoC, the QoS is achieved by exploiting the signal pressure embedded into the NTTP packet definition (Figures 11.1 and 11.2). The pressure

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed. For example, we can imagine associating the generation of the pressure signal when a certain threshold has been reached in the FIFO of the corresponding IP. This pressure information will be embedded in the NTTP packet at the NIU level: packets that have pressure bits equal to zero will be considered without QoS; packets with a nonzero value of the pressure bit will indicate preferred traffic class.* Such a QoS mechanism offers immediate service to the most urgent inputs and variables, and fair service whenever there are multiple contending inputs of equal urgency (BE). Within switches, arbitration decisions favor preferred packets and allocate remaining bandwidth (after preferred packets are served) fairly to contending packets. When there are contending preferred packets at the same pressure level, arbitration decisions among them are also fair. The Arteris NoC supports the following four different traffic classes:

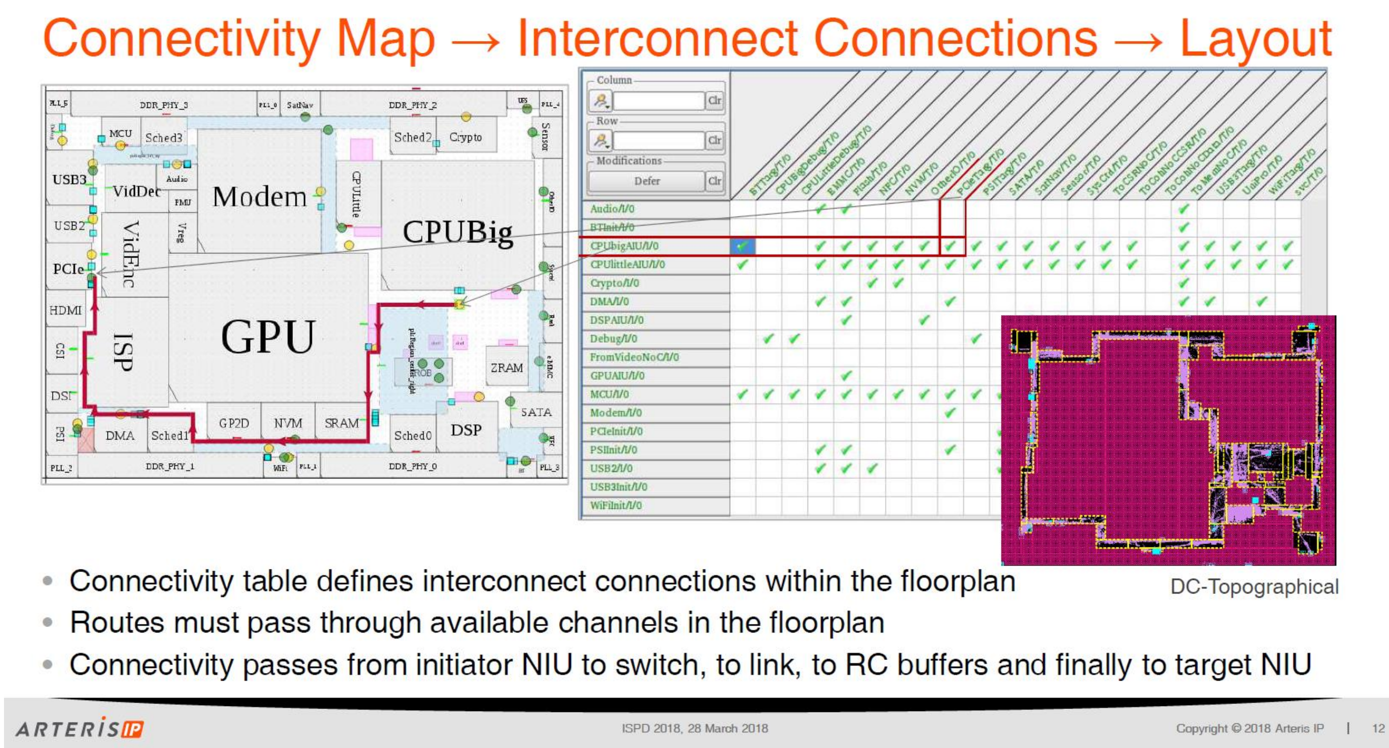
'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	• **Real time and low latency (RTLL)**—Traffic flows that require the lowest possible latency. Sometimes it is acceptable to have brief intervals of longer latency as long as the average latency is low. Care must be taken to avoid starving other traffic flows as a side effect of pursuing low latency. • **Guaranteed throughput (GT)**—Traffic flows that must maintain their throughput over a relatively long time interval. The actual bandwidth needed can be highly variable even over long intervals. Dynamic pressure is employed for this traffic class. • **Guaranteed bandwidth (GBW)**—Traffic flows that require a guaranteed amount of bandwidth over a relatively long time interval. Over short periods, the network may lag or lead in providing this bandwidth. Bandwidth meters may be inserted onto links in the NoC to regulate these flows, using either of the two methods. If the flow is assigned high pressure, the meter asserts backpressure (flow control) to prevent the flow from exceeding a maximum bandwidth. Alternatively, the meter can modulate the flows pressure (priority) dynamically as needed to maintain an average bandwidth. • **Best effort (BE)**—Traffic flows that do not require guaranteed latency or throughput but have an expectation of fairness.

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	* Note that in the NTTP packet, the pressure field allows more then one bit, resulting in multiple levels of preferred traffic.

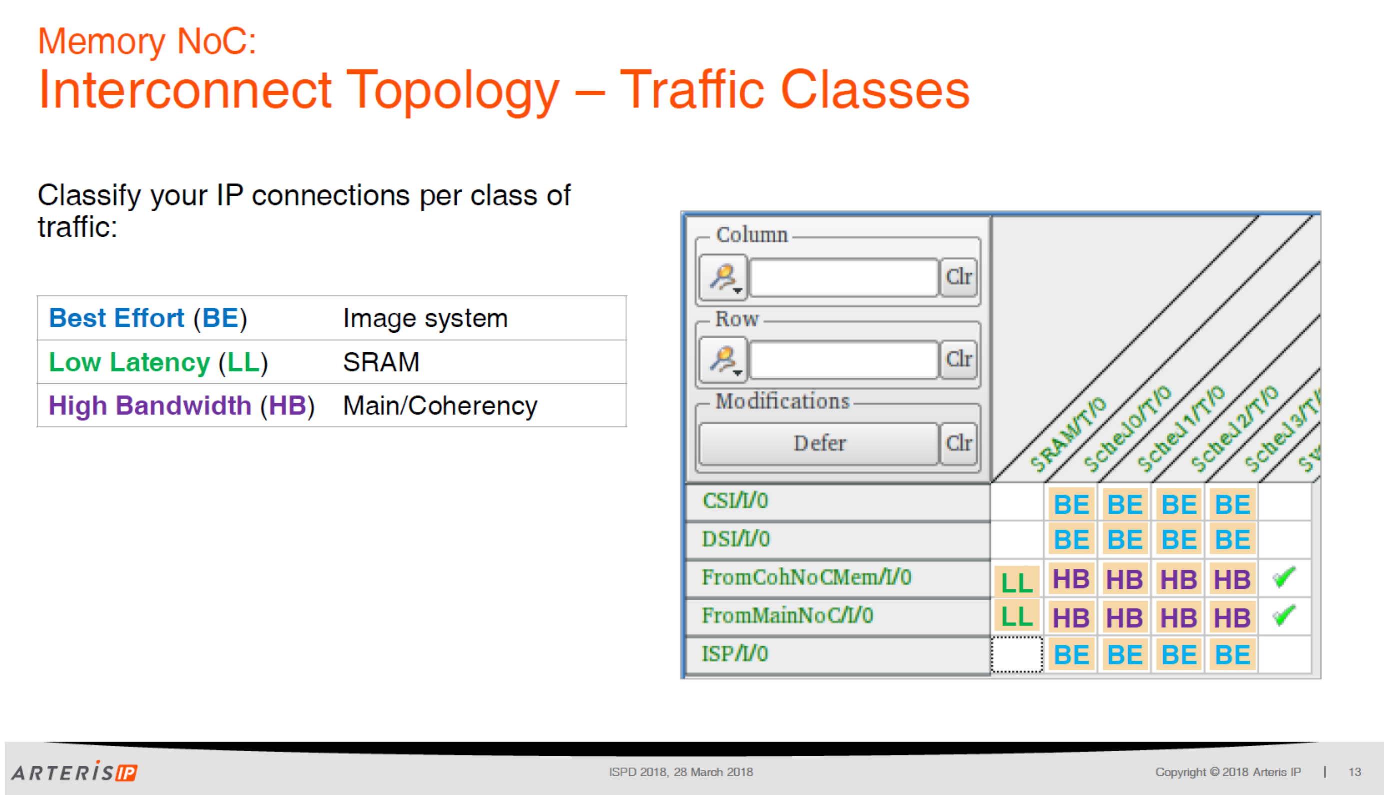
Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 315-316.

Connections within the Arteris NoC interconnect may be defined by a connectivity table:



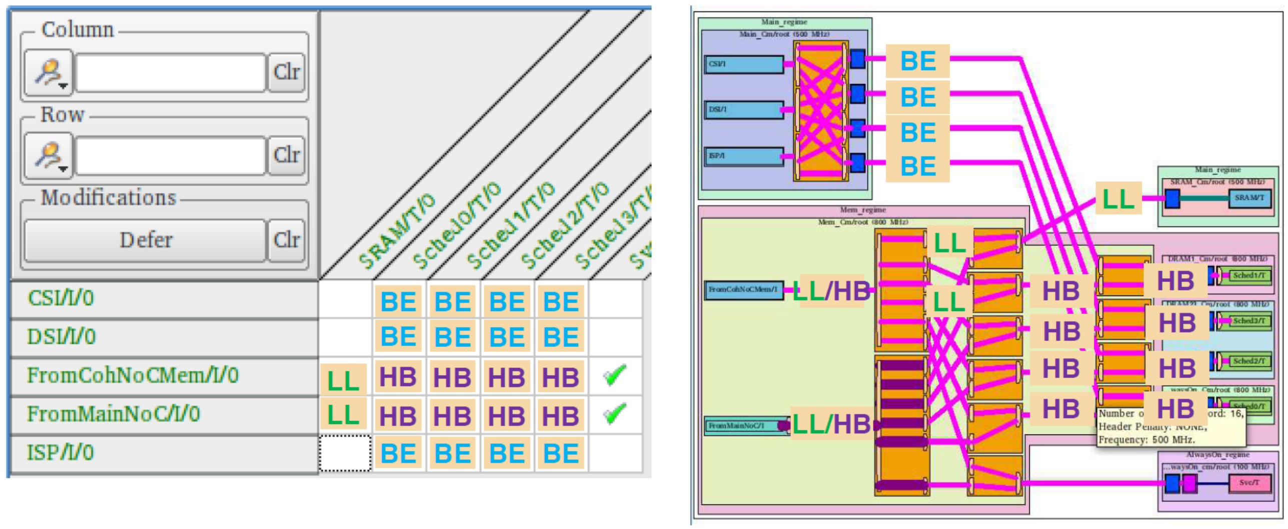
4893-4043-7313.3

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12. As a further illustration, connections within the Arteris NoC may be classified by traffic class and traffic classes, including related to, for example, latency, may be mapped onto the Arteris interconnect topology:



U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

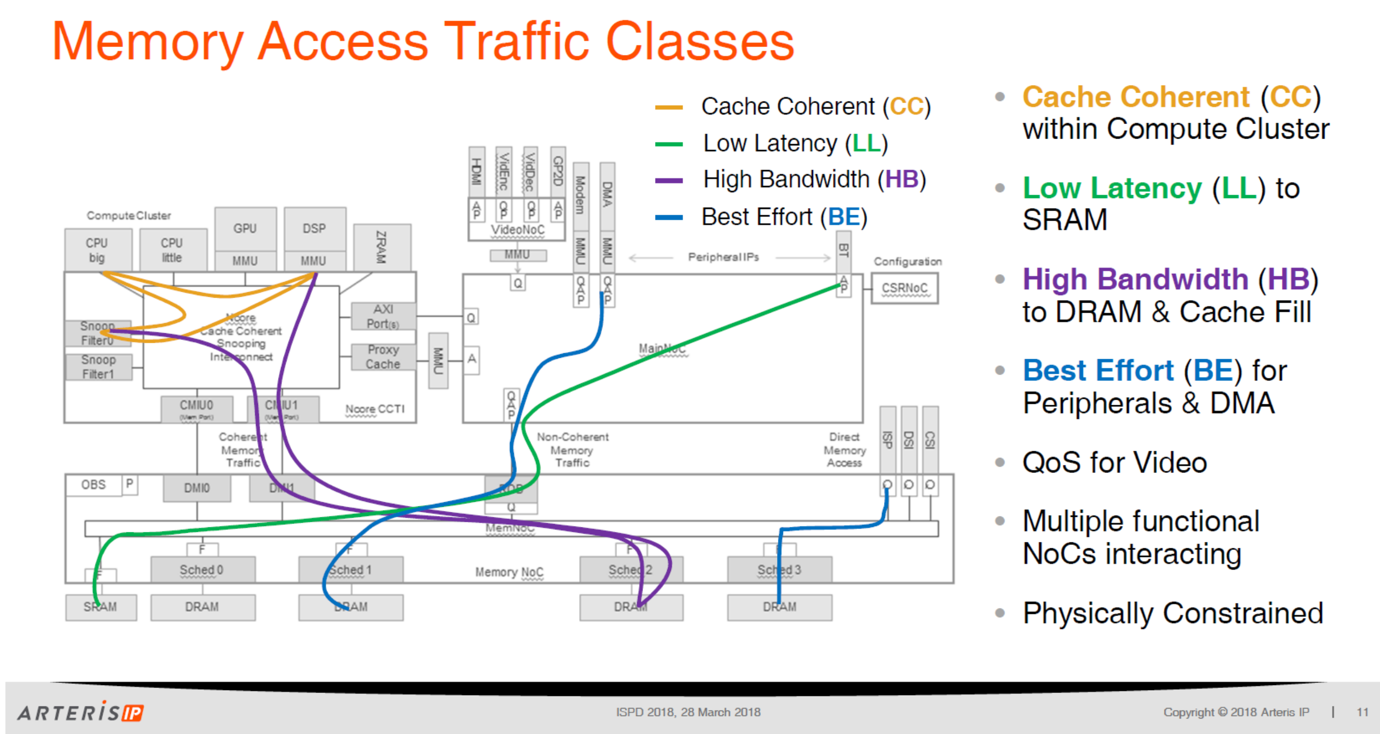
'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	Memory NoC: Traffic classes are mapped onto logical interconnect topology



ARTERIS IP ISPD 2018, 28 March 2018 Copyright © 2018 Arteris IP | 16

4893-4043-7313.3

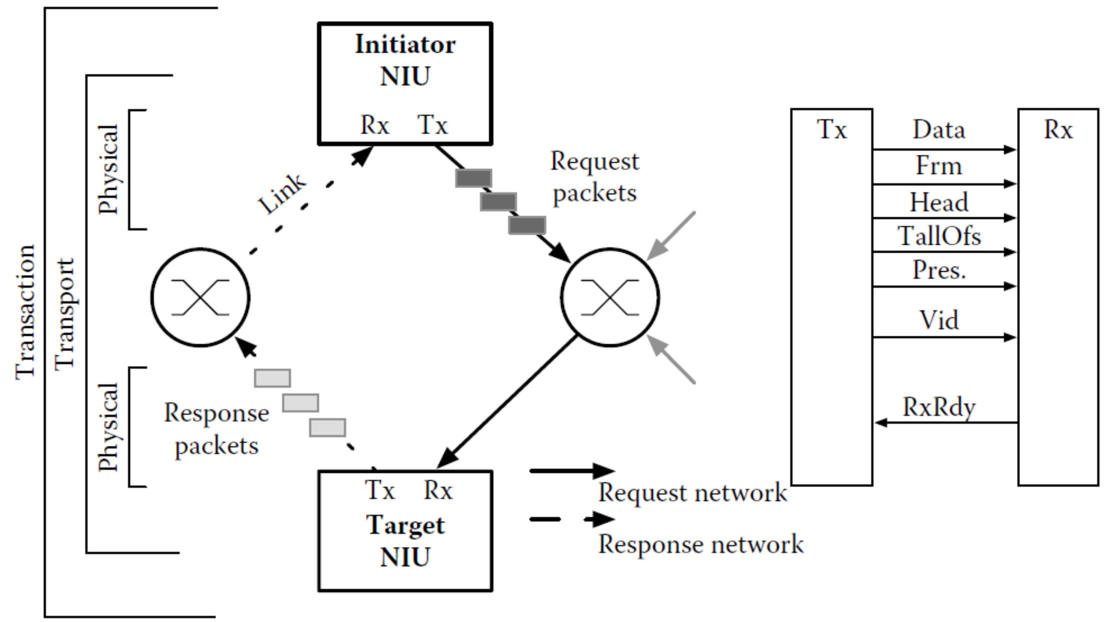
U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

<table>
<tr><th>'052 Patent Claim</th><th>Lenovo Product Including Snapdragon System on Chip[1]</th></tr>
<tr><td></td><td>


See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slides 11, 13, 16.</td></tr>
<tr><td>controlling the communication between said at least one first of said plurality of</td><td>The Arteris NoC utilized by the Snapdragon SoC included in the Lenovo product controls the communication between said at least one first of said plurality of processing modules (M) and said interconnect means (N) by at least one network interface (NI) associated to said at least one first of said processing modules, either literally or under the doctrine of equivalents.</td></tr>
</table>

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
processing modules (M) and said interconnect means (N) by at least one network interface (NI) associated to said at least one first of said processing modules,	For example, the Arteris NoC used by the Snapdragon SoC included in the Lenovo product has "Network Interface Units (NIU) connecting IP blocks to the network" with "[i]nterface units for OCP, AMBA AHB, APB, and AXI protocols […] provided." Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311. In the Arteris NoC, "[t]ransaction layer services are provided to the nodes at the periphery of the NoC by special units called Network Interface Units (NIUs)." *Id.* In the Arteris NoC, "[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network…. Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path."

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

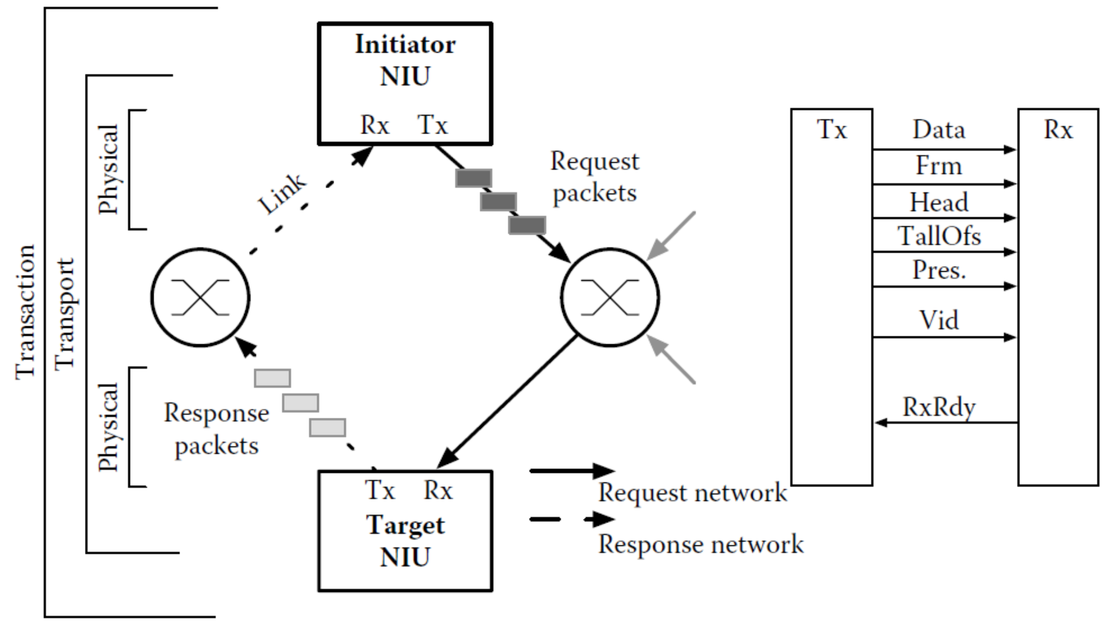
'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	 **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313. In the Arteris NoC, "transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols":

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	11.3.1.1 Transaction Layer The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network. *Id.* at 312-313.

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
mapping the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification.	The Arteris NoC utilized by the Snapdragon SoC included in the Lenovo product maps the requested at least one communication service based on said specific communication properties to a connection based on a set of connection properties according to said at least one communication service identification, either literally or under the doctrine of equivalents. For example, in the Arteris NoC used by the Snapdragon SoC included in the Lenovo product, "[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network…. Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path."

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	 **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312-313. As a further illustration, the "Arteris NTTP protocol is packet-based" and the packets, which have "header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address," are "transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes":

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	11.3.1.2 Transport Layer The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target. *Id.* at 313. As yet a further illustration, packets in the Arteris NoC are "delivered as words that are sent along links and "[o]ne link (represented in Figure 11.1) defines the following signals," which include "the current priority of the packet used to define preferred traffic class (or Quality of Service)" and "[f]low control":

4893-4043-7313.3

	maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in Figure 11.1) defines the following signals: • **Data**—Data word of the width specified at design-time. • **Frm**—When asserted high, indicates that a packet is being transmitted. • **Head**—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only. • **TailOfs**—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only. • **Pres.**—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2). • **Vld**—Data valid: when asserted high, indicates that a word is being transmitted. • **RxRdy**—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy. This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTTP communications.

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	Id. at 313-314. As a further example, the packets sent in the Arteris NoC are "composed of cells that are organized into fields, with each field carrying specific information," including "Pres," "Slave address" and "Slave offset":

Field	Size	Function
Opcode	4 bits/3 bits	Packet type: 4 bits for requests, 3 bits for responses
MstAddr	User Defined	Master address
SlvAddr	User Defined	Slave address
SlvOfs	User Defined	Slave offset
Len	User Defined	Payload length
Tag	User Defined	Tag
Prs	User defined (0 to 2)	Pressure
BE	0 or 4 bits	Byte enables
CE	1 bit	Cell error
Data	32 bits	Packet payload
Info	User Defined	Information about services supported by the NoC
Err	1 bit	Error bit

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]

StartOfs	2 bits	Start offset
StopOfs	2 bits	Stop offset
WrpSize	4 bits	Wrap size
Rsv	Variable	Reserved
CtlId	4 bits/3 bits	Control identifier, for control packets only
CtlInfo	Variable	Control information, for control packets only
EvtId	User defined	Event identifier, for event packets only

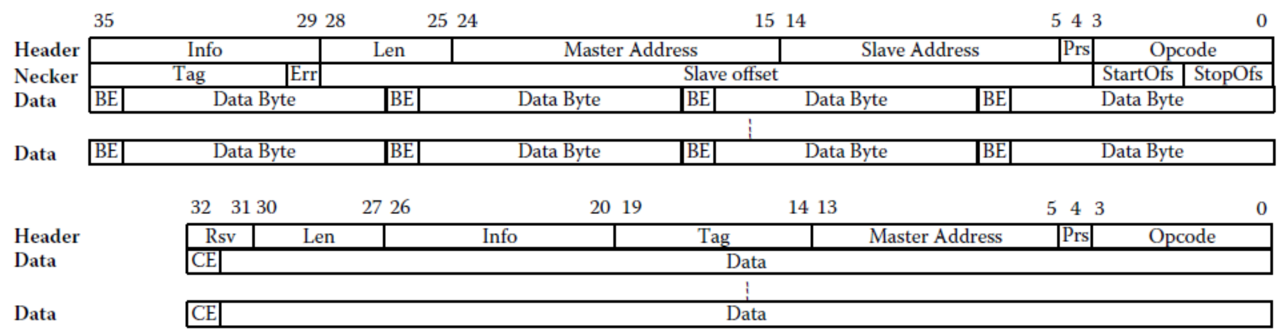


FIGURE 11.2
NTTP packet structure.

Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313, 314-315.

4893-4043-7313.3

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	As further illustration, "[f]or the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2)." *Id.* at 318. As a further illustration, the Arteris NoC implements Quality of Service (QoS) to "provide[] a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic"; QoS, which includes guarantees of, for example, throughput and/or latency, "is achieved by exploiting the signal pressure embedded into the NTTP packet definition" where the "pressure signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed"; and the "pressure information will be embedded in the NTTP packet at the NIU level": **Quality of Service (QoS).** The QoS is a very important feature in the interconnect infrastructures because it provides a regulation mechanism allowing specification of guarantees on some of the parameters related to the traffic. Usually the end users are looking for guarantees on bandwidth and/or end-to-end communication latency. Different mechanisms and strategies have been proposed in the literature. For instance, in Æthereal NoC [11,24] proposed by NXP, a TDMA approach allows the specification of two traffic categories [25]: BE and GT. In the Arteris NoC, the QoS is achieved by exploiting the signal pressure embedded into the NTTP packet definition (Figures 11.1 and 11.2). The pressure

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	signal can be generated by the IP itself and is typically linked to a certain level of urgency with which the transaction will have to be completed. For example, we can imagine associating the generation of the pressure signal when a certain threshold has been reached in the FIFO of the corresponding IP. This pressure information will be embedded in the NTTP packet at the NIU level: packets that have pressure bits equal to zero will be considered without QoS; packets with a nonzero value of the pressure bit will indicate preferred traffic class.* Such a QoS mechanism offers immediate service to the most urgent inputs and variables, and fair service whenever there are multiple contending inputs of equal urgency (BE). Within switches, arbitration decisions favor preferred packets and allocate remaining bandwidth (after preferred packets are served) fairly to contending packets. When there are contending preferred packets at the same pressure level, arbitration decisions among them are also fair. The Arteris NoC supports the following four different traffic classes:

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	• **Real time and low latency (RTLL)**—Traffic flows that require the lowest possible latency. Sometimes it is acceptable to have brief intervals of longer latency as long as the average latency is low. Care must be taken to avoid starving other traffic flows as a side effect of pursuing low latency. • **Guaranteed throughput (GT)**—Traffic flows that must maintain their throughput over a relatively long time interval. The actual bandwidth needed can be highly variable even over long intervals. Dynamic pressure is employed for this traffic class. • **Guaranteed bandwidth (GBW)**—Traffic flows that require a guaranteed amount of bandwidth over a relatively long time interval. Over short periods, the network may lag or lead in providing this bandwidth. Bandwidth meters may be inserted onto links in the NoC to regulate these flows, using either of the two methods. If the flow is assigned high pressure, the meter asserts backpressure (flow control) to prevent the flow from exceeding a maximum bandwidth. Alternatively, the meter can modulate the flows pressure (priority) dynamically as needed to maintain an average bandwidth. • **Best effort (BE)**—Traffic flows that do not require guaranteed latency or throughput but have an expectation of fairness.

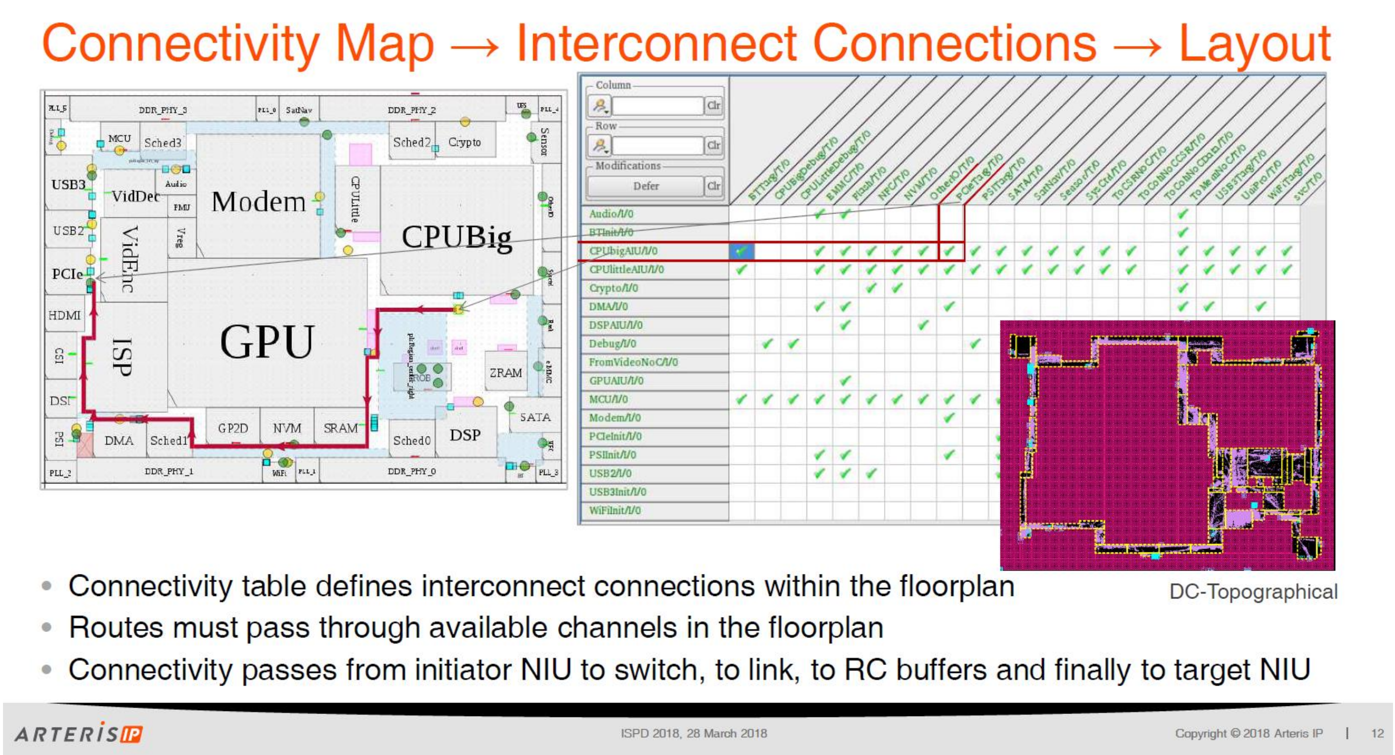
U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]

* Note that in the NTTP packet, the pressure field allows more then one bit, resulting in multiple levels of preferred traffic.

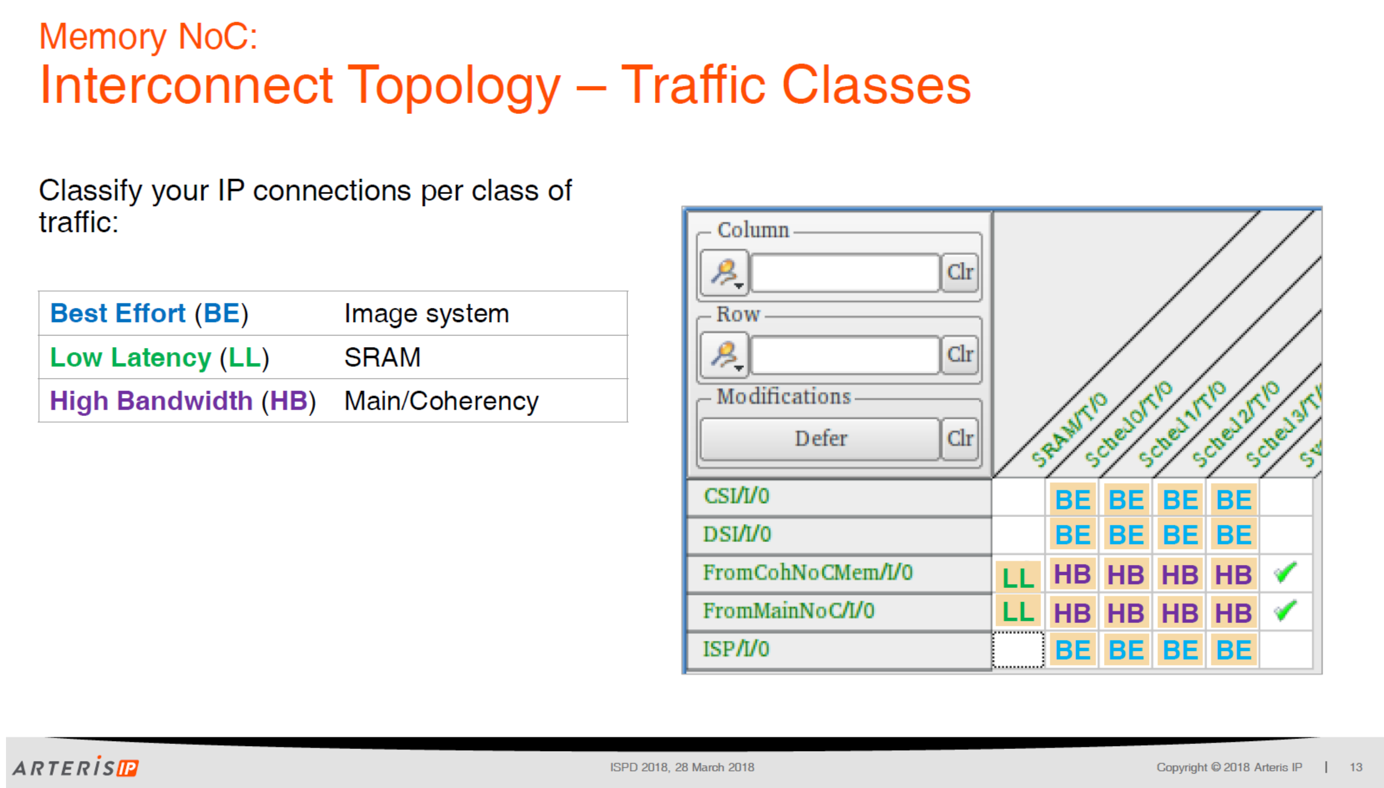
Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 315-316.

Connections within the Arteris NoC interconnect may be defined by a connectivity table:



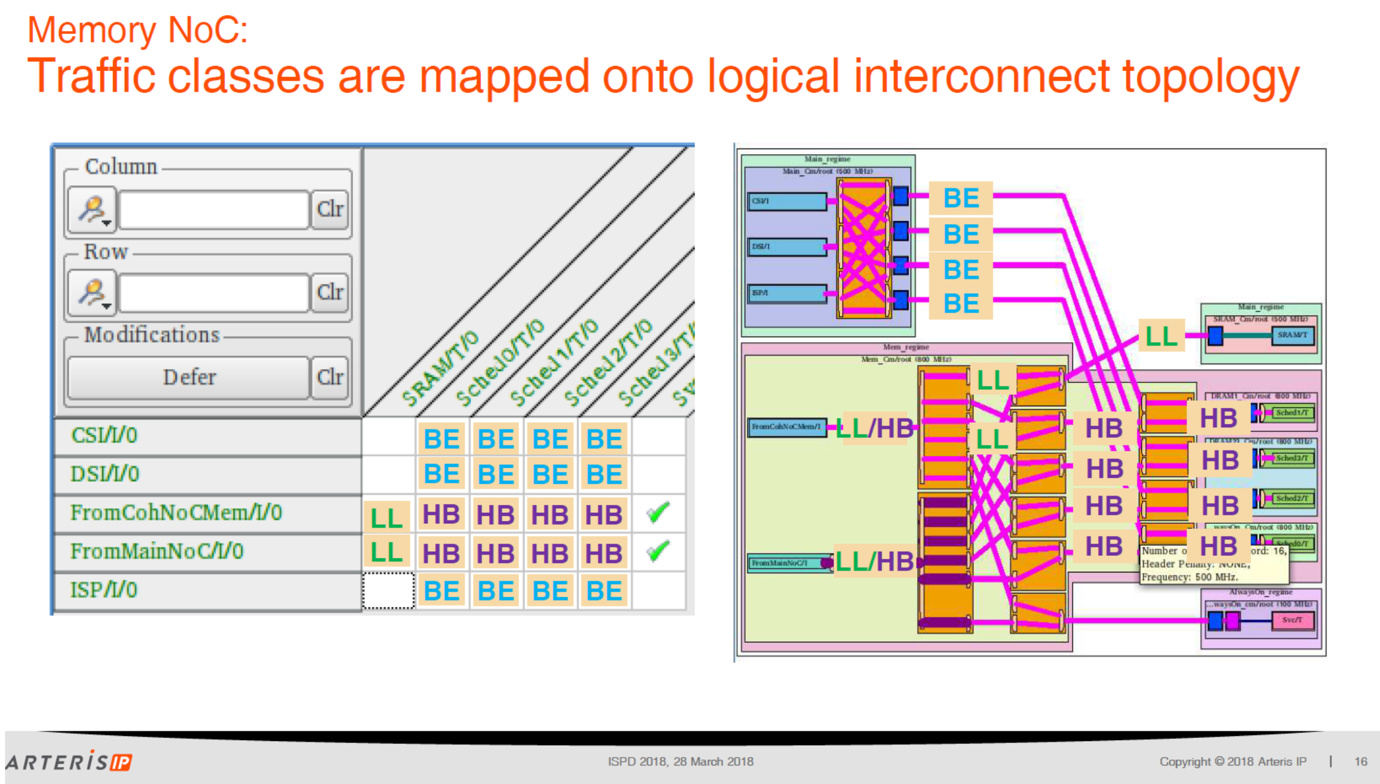
4893-4043-7313.3

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 12. As a further illustration, connections within the Arteris NoC may be classified by traffic class and traffic classes, including related to, for example, latency, may be mapped onto the Arteris interconnect topology: 

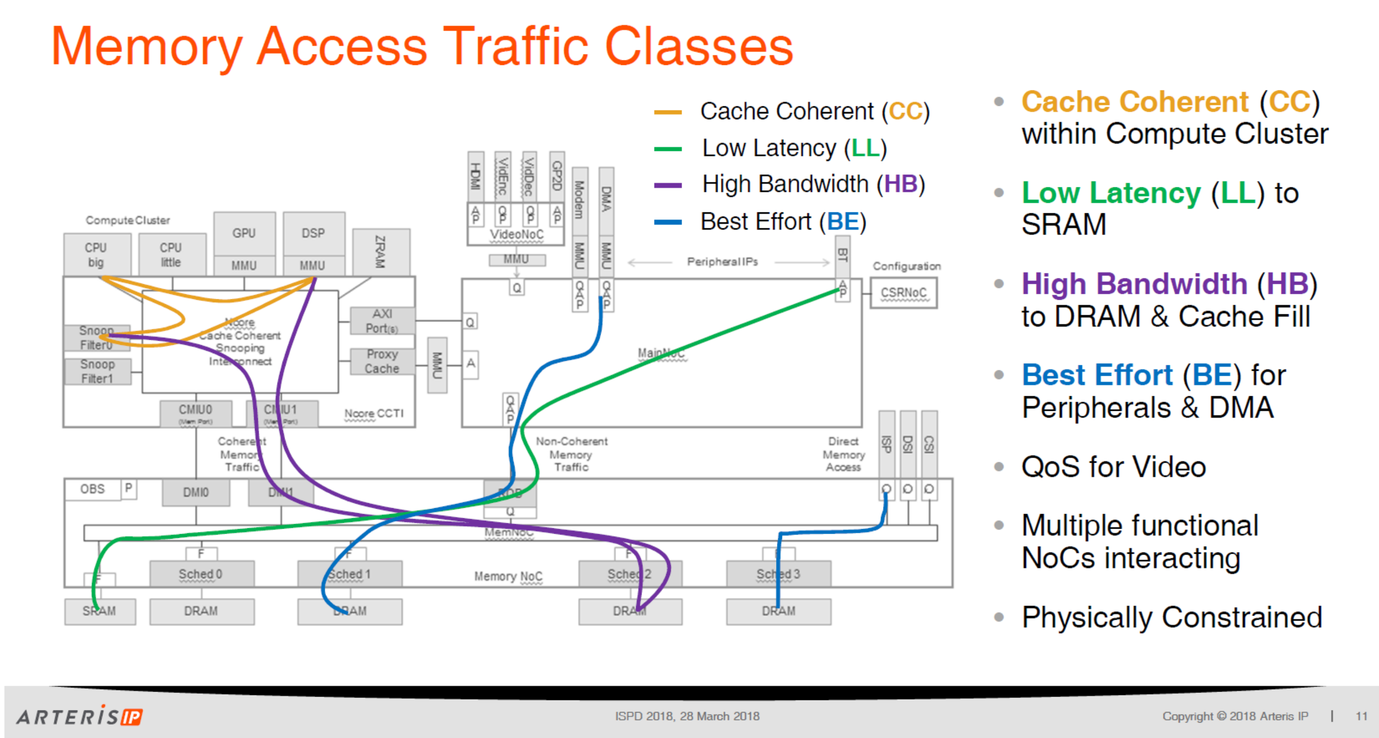
4893-4043-7313.3

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]
	

U.S. Patent No. 7,594,052 (Radulescu & Goossens)
"Integrated circuit and method of communication service mapping"

'052 Patent Claim	Lenovo Product Including Snapdragon System on Chip[1]



See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slides 11, 13, 16.

4893-4043-7313.3